(19) Japan Patent Office (JP)
(11) Patent Application Disclosure No: H3-187215
(12) Patent Disclosure Report (A)

(43) Disclosure Date: August 15, 1991

(51) Int. Cl.[5] Identification No. Intra-office Filing No.
H 01 L 21/205 7739-5F

Examination Request: Not yet requested
Number of claims: 1
(Total of 3 pages)

(54) Title of Invention: Silicon Thin Film Manufacturing Method

(21) Patent Application: H1-326740

(22) Date of Application: December 15, 1989

(72) Inventor: Takashi Ueda
c/o Sharp Co., Ltd.
22-22 Nagaike-cho, Abeno-ku, Osaka City, Osaka Prefecture

(71) Applicant: Sharp Co., Ltd.
22-22 Nagaike-cho, Abeno-ku, Osaka City, Osaka Prefecture

(74) Agent: Shintaro Nogawa, Attorney

Specifications

1. Title of invention

Silicon Thin Film Manufacturing Method

2. Range of Patent Claims

1. A silicon thin film manufacturing method characterized by arranging a substrate in a pressure-reduction CVD device, allowing gaseous phase growth of silicon at a growth rate of 60 Å/minute or less on said substrate by heating the interior of the device to 400-550°C and supplying substantially pure disilane (Si_2H_6) therein, and by forming a silicon thin film having a film thickness of 300 Å or less.

3. Detailed Description of the Invention

(A) Field of Industrial Utilization

This invention is related to a manufacturing method of silicon thin film. The manufacturing method of this invention is suitably used to manufacture thin film transistors.

(B) Prior Art

In the past, thin film transistors (TFT) have been used in load elements within liquid crystal display drive transistors and driver circuits, and in static RAM (SRAM) memory cells, and these TFTs were formed using silicon thin film accumulating by a gaseous phase growth method. Silicon thin film is produced by allowing gaseous phase growth of monosilane (SiH_4) as the principal material. The gaseous phase growth conditions are as follows:

Accumulation Temperature:	620°C
Accumulation Rate:	90 Å/min
Pressure:	0.38 Torr (50 Pa)
SiH_4 Flow Rate:	100 sccm
Device:	pressure reduction CVD device
N_2 Flow Rate:	300 sccm

(C) Problems to be solved by the invention

The reduction of TFT current leakage is a specific requirement in SRAM devices. When making an Si thin film comprising TFTs thin, it is necessary to make the silicon film thickness thin in order to reduce current leakage because joint current leakage can be reduced by:

(1) Increasing the OFF resistance of the channel part, and
(2) Reducing the surface area of the joint part. It is preferable to have a film thickness of 300 Å or less.

However, when using this conventional technology to form a thin film of 300 Å or less, silicon layer 13 grows in an island shape on the surface of substrate 12 as indicated in Figure 4, and there is the problem that continuity of the thin film cannot be obtained.

This invention is a method to resolve the aforementioned problem, and offers a silicon thin film formation method that can form continuous silicon thin film with a film thickness of 300 Å or less without making island-shaped gaps.

(D) Means to Resolve the Problems

This invention offers a silicon thin film manufacturing method characterized by arranging a substrate in a pressure-reduction CVD device, allowing gaseous phase growth of silicon at a growth rate of 60 Å/minute or less on said substrate by heating the interior of the device to 400-550°C and supplying substantially pure disilane (Si_2H_6) therein, and by forming a silicon thin film having a film thickness of 300 Å or less.

The disilane in this invention is a substance for the purpose of forming a silicon thin film having a film thickness of 300 Å or less, and can be used by supplying substantially pure disilane (Si_2H_6) into the CVD device. This disilane uses a substance that substantially contains no monosilane, trisilane or any other silane. This disilane may be supplied using only disilane, but it may also be supplied by diluting with a gas, for example, nitrogen, hydrogen, helium, or argon. The supply rate varies depending on the capacity of the CVD device, and because the gaseous phase growth rate of the silicon thin film increases as the supply rate increases at the same capacity, [the CVD device] is set up such that the gaseous phase growth rate is one in which a silicon thin film with a film thickness of 300 Å or less can be grown with satisfactory control.

The aforementioned substrate is a substance for the purpose of manufacturing a silicon thin film on it, and a semiconductor or an insulating body can be used as the substrate. For example, when manufacturing TFT, it is possible to use a silicon substrate in which the surface is covered with an insulating film and elements have been formed.

In this invention, the interior of the device is heated to 400-550°C. This addition of heat is for the purpose of decomposing the disilane at a specific rate and converting it to silicon. Normally, 400-550°C is preferable, and 450-500°C is optimum. If the heating temperature exceeds 550°C the decomposition rate of the disilane becomes rapid, and it becomes difficult to control the film thickness of the silicon thin film obtained. If the heating temperature is less than 400°C, the decomposition rate of the disilane becomes too slow, and this is not preferable. It is best to set the decomposition rate of the aforementioned disilane such that the gaseous phase growth rate of the silicon thin film on the substrate is 60 Å/min or less. If the gaseous phase growth rate is 60 Å/min or more, it becomes difficult to control the film thickness of the silicon thin film to be 300 Å or less, and this is not preferable. Silicon thin film having a film thickness of 300 Å or less can be satisfactorily used in, for example, TFTs, polysilicon load resistors, etc.

(E) Action

Uniform gaseous phase growth of silicon is allowed on a substrate by decomposing disilane at a specific temperature in a pressure reduction CVD device.

(F) Embodiments

Preparation of the Substrate

As indicated in Figure 1, gate electrodes 2 are formed on silicon substrate 1 using ordinary MOS processing. Bulk Nch bulk transistors 2A are formed by doping impurities into the silicon substrate. A silicon oxide film 3 (film thickness 500 Å) is formed on this using the CVD method, and the substrate is prepared by opening contact holes 4 using the hot etch method.

Preparation of Silicon Thin Film

The aforementioned substrate is arranged in a pressure reduction CVD device heated to 450°C, and a vacuum of 10^{-3} Torr or less is drawn in the device. Next, disilane (manufactured by Toa Chemical Industries Co., Ltd., purity 99.99%) is supplied into the device at a flow rate of

200 sccm, and N_2 gas is supplied at a flow rate of 300 sccm. The pressure inside the device is controlled at 0.38 Torr (50 Pa), and gaseous phase growth (growth rate 6 Å/min) of silicon on the substrate is allowed. Gaseous phase growth is conducted for 30 minutes, and silicon thin film 5 having a film thickness of 180 Å is formed as indicated in Figure 2.

It was confirmed that this silicon thin film was a uniform, continuous film without the formation of any island-shaped gaps.

SRAM Memory Cell Preparation

Next, as indicated in Figure 3, a SRAM memory cell was formed by using photolithography to etch a specific pattern on the aforementioned silicon thin film, by forming gate electrode 8 thereon close to gate insulating film 6, and by forming source and drain 5' by embedding impurities in a specific region of the aforementioned silicon thin film. Here, 9 and 10 are insulating films, and 11 is a metal routing layer. The SRAM memory cell obtained has superior memory characteristics and hardly any current leakage.

(G) Effect of the Invention

According to this invention it is possible to offer a silicon thin film formation method that can form a continuous thin film with a film thickness of 300 Å or less without any island-shaped gaps.

By using this method, it is possible to prepare a highly reliable thin film transistor in which the current leakage has been greatly reduced.

4. Brief Explanation of the Diagrams

Figures 1 through 3 are diagrams to explain the manufacturing processes of silicon thin film prepared in an embodiment of this invention. Figure 4 is a diagram to explain a conventional silicon thin film.

1	Silicon substrate
2	Gate electrode
2A	Bulk transistor
3	Silicon oxide film
4	Connector hole
5	Silicon thin film
5'	Source, drain
6	Gate insulating film
8	Gate electrode
9, 10	Insulating layer
11	Metal routing layer

Agent: Shintaro Nogawa, Attorney [Seal:} Shintaro Nogawa

Figure 1
[see source for figure]

Figure 2
[see source for figure]

Figure 3
[see source for figure]

Figure 4
[see source for figure]